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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/025,331	12/19/2001	Gregg A. Bouchard	2-3-1	8231

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Ryan, Mason & Lewis, LLP
90 Forest Avenue
Locust Valley, NY 11560

EXAMINER	
TRUONG, BAO Q	
ART UNIT	**PAPER NUMBER**
2187	

DATE MAILED: 12/09/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/025,331	BOUCHARD ET AL.	
	Examiner	Art Unit	
	Bao Q Truong	2187	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *19 December 2001*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-19* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,2,5-7 and 10-19* is/are rejected.

7)☒ Claim(s) *3,4,8 and 9* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *19 December 2001* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

1. The instant application having Application No. 10/025,331 has a total of 19 claims pending in the application; there are 4 independent claims and 15 dependent claims, all of which are ready for examination by the examiner.

Oath/Declaration

2. The applicant's oath/declaration has been reviewed by the examiner and is found to conform to the requirements prescribed in 37 C.F.R. § 1.63.

Drawings

3. The applicant's drawings submitted are acceptable for examination purposes.

Specification

4. Applicant is reminded of the proper language and format for an abstract of the disclosure.

The abstract should be in narrative form and generally limited to a single paragraph on a separate sheet within the range of 50 to 150 words. It is important that the abstract not exceed 150 words in length since the space provided for the abstract on the computer tape used by the printer is limited. The form and legal phraseology often used in patent claims, such as "means" and "said," should be avoided. The abstract should describe the disclosure sufficiently to assist readers in deciding whether there is a need for consulting the full patent text for details.

The language should be clear and concise and should not repeat information given in the title. It should avoid using phrases which can be implied, such as, "The disclosure concerns," "The disclosure defined by this invention," "The disclosure describes," etc.

5. The abstract of the disclosure is objected to because it is not within the range of 50 to 150 words. Correction is required. See MPEP § 608.01(b).

6. The disclosure is objected to because of the following informalities: second paragraph, page 7, recites "banks B0, B1 and B3 of the N banks". Fig. 2, however, shows only banks B0, B1 and B2. Appropriate correction is required.

Claim Rejections - 35 USC § 102

7. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

8. Claims are rejected under 35 U.S.C. 102(e) as being anticipated by Waters et al. (U.S. Patent No. 6,430,527 B1).

Referring to claim 1, Waters discloses a memory system comprising:

a memory controller as a search engine being able to control a memory chip (see figure 7: element 35; figure 15; and column 10: lines 4-7); and

a plurality of memory banks operatively coupled to the memory controller (see figure 7: elements 39-40), each of the memory banks configured for storing a plurality of data items, wherein a given data item is stored as multiple copies of the data item with a given one of the multiple copies in each of a designated minimum number of the memory banks as storing a copy of all internal nodes of the augmented tree in two memory banks to optimize bandwidth (see Abstract; column 9: lines 57-59; and column 10: lines 20-38);

the memory controller being adapted to process requests for access to the data items stored in the memory banks in accordance with a specified bank access sequence configured to prevent bank conflict between the access requests as the search engine performing tree searches by alternating banks (see figure 9 and column 10: lines 34-38).

As to claim 2, Waters further discloses that the minimum number of the memory banks for storage of the multiple copies of the given data item is determined as a function of a random cycle time of the memory banks (see figures 8-9 and column 10: lines 20-38).

As to claim 5, Waters further discloses that each of at least a subset of the plurality of memory banks is configured to store the same plurality of data items, the subset comprising at least two of the memory banks as two banks of a memory chip are configured to store a copy of all internal nodes of the augmented tree (see column 9: lines 53-59).

As to claim 6, Waters further discloses that the system comprises a first memory channel including the plurality of memory banks as a first plurality of memory banks and a second memory channel including a second plurality of memory banks as different SDRAM chips (see figure 7: elements SDRAM Chips).

As to claim 7, Waters further discloses that the memory controller further comprises a first controller coupled to each of the first plurality of memory banks via a first set of address, data and control bus, and a second controller coupled to each of the second plurality of memory banks via a second set of address, data and control bus as different search engines being able to control a memory chip (see figure 7: element 35; figure 15; and column 10: lines 4-7).

As to claim 10, Waters further discloses that each of at least a subset of the plurality of memory banks is implemented using one or more dynamic random access memory (DRAM) devices as SDRAM (see figure 7: element 38).

As to claim 12, Waters further discloses that the memory system being operable in multiple modes, the multiple modes comprising at least:

a first mode in which a given data item is stored as multiple copies of the data item with a given one of the multiple copies in each of a designated minimum number of the memory bank as storing a copy of all internal nodes of the augmented tree in two memory banks to optimize bandwidth (see figure 7: elements 39-40; figure 9; Abstract; column 9: lines 57-59; and column 10: lines 20-38), and the memory controller is adapted to process requests for access to the data

items stored in the memory banks in accordance with the specified bank access sequence as the search engine performing tree searches by alternating banks with a 100% duty factor (see figure 9 and column 10: lines 34-38); and

a second mode in which the given data item is stored as a single copy of the data item with a single copy in a particular one of the plurality of memory bank as storing a copy of all internal nodes of the augmented tree in a single memory bank (see column 10: lines 20-23), and the memory controller is adapted to process requests for access to the data items stored in the memory banks in accordance with a sequence other than the specified bank access sequence as the search engine performing tree searches by from a single bank with a 50% duty factor (see figure 8 and column 10: lines 20-24).

As to claims 13 and 14, Waters further discloses that the access requests comprise a plurality of read requests and a plurality of write requests, the read requests and the write requests being in an unbalanced ratio favoring the read requests as the memory banks are more frequently accessed with read operations during tree searches and are less frequently accessed with write operations during initialization and updates (see column 9: lines 49-52).

Referring to claim 15, Waters discloses a processing system comprising:

a processing device as a device sending "input packet descriptors" to a search ASIC (see figure 7); and

a memory system operatively coupled to the processing device (see figure 7), the memory system comprising:

a memory controller as a search engine being able to control a memory chip (see figure 7: element 35; figure 15; and column 10: lines 4-7); and

a plurality of memory banks operatively coupled to the memory controller (see figure 7: elements 39-40), each of the memory banks configured for storing a plurality of data items, wherein a given data item is stored as multiple copies of the data item with a given one of the multiple copies in each of a designated minimum number of the memory banks as storing a copy of all internal nodes of the augmented tree in two memory banks to optimize bandwidth (see Abstract; column 9: lines 57-59; and column 10: lines 20-38);

the memory controller being adapted to process requests for access to the data items stored in the memory banks in accordance with a specified bank access sequence configured to prevent bank conflict between the access requests as the search engine performing tree searches by alternating banks (see figure 9 and column 10: lines 34-38).

As to claim 16, Waters further discloses that the processing device comprises a network processor as a device sending "input packet descriptors" to a search ASIC used in net working to route packet (see figure 7 and column 1: lines 13-16).

As to claim 17, Waters furthers discloses that the memory system implements an external tree memory for the network processor as the memory banks are used to stored tree data structure for packet prefix searching (see figures 1-4 and Abstract).

Referring to claim 18, Waters teaches a method for use in a memory system comprising a memory controller as a search engine being able to control a memory chip (see figure 7: element 35) and a plurality of memory banks (see figure 7: elements 39-40) operatively coupled to the memory controller, each of the memory banks configured for storing a plurality of data items, the method comprising:

storing a given data item as multiple copies of the data item with a given one of the multiple copies in each of a designated minimum number of the memory banks as storing a copy of all internal nodes of the augmented tree in two memory banks to optimize bandwidth (see Abstract; column 9: lines 57-59; and column 10: lines 20-38); and

processing in the memory controller requests for access to the data items stored in the memory banks in accordance with a specified bank access sequence configured to prevent bank conflict between the access requests as the search engine performing tree searches by alternating banks (see figure 9 and column 10: lines 34-38).

Referring to claim 19, Waters teaches a method for use in a memory system comprising a memory controller and a plurality of memory banks operatively coupled to the memory controller, each of the memory banks configured for storing a plurality of data items, the method comprising:

determining a minimum number of the memory banks for storage of multiple copies of a given data item as a function of a random cycle time of the memory banks as a 50% duty factor is obtained by storing a copy of all internal nodes of the augmented tree in one memory bank; a 100% duty factor is obtained by storing a copy of all internal nodes of the augmented tree in two

memory banks (see figures 8-9; Abstract; column 9: lines 57-59; and column 10: lines 20-38); and

storing a given data item as multiple copies of the data item with a given one of the multiple copies in each of a designated minimum number of the memory banks as storing a copy of all internal nodes of the augmented tree in two memory banks to optimize bandwidth (see Abstract; column 9: lines 57-59; and column 10: lines 20-38).

Claim Rejections - 35 USC § 103

9. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

10. Claim 11 is rejected under 35 U.S.C. 103(a) as being unpatentable over Waters et al. (U.S. Patent No. 6,430,527 B1) in view of Ohshima et al. (U.S. Patent No. 6,636,445 B2).

As to claim 11, Waters discloses all the limitations of claim 10 above. However, Waters does not disclose that one or more of the DRAM device comprises a fast cycle DRAM device.

Ohshima discloses a fast cycle DRAM device (see figure 1 and Background of The Invention) to be used in network field, i.e. routers or LAN switches (see column 1: lines 46-53).

It would have been obvious to one having an ordinary level of skill in the art at the time the invention was made to modify the apparatus disclosed by Waters so that one or more of the DRAM device comprises a fast cycle DRAM device. This would have been obvious because Ohshima discloses that fast cycle DRAM devices provide high-speed data transferring for routers and LAN switches (see column 1: lines 46-53).

Allowable Subject Matter

11. Claims 3-4 and 8-9 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Conclusion

12. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. See Form PTO-892.

13. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Bao Q Truong whose telephone number is (571) 272-4202. The examiner can normally be reached on Monday-Friday from 6:00 AM to 3:00 PM (ET).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Donald A Sparks, can be reached on (571) 272-4201. The fax phone number for the organization where this application or proceeding is assigned is (703) 746-7239.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (571) 272-2100.

BAO QUE TRUONG

BT

Patent Examiner

6 December 2004

Donald Sparks

Supervisory Patent Examiner

Technology Center 2100